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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,984	02/04/2002	Tse-Yu Yeh	5580-04403	4187

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EXAMINER	
RIZZUTO, KEVIN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,984	YEH ET AL.	
	Examiner	Art Unit	
	Kevin P. Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 21-28 have been examined.

2. Acknowledgement of papers filed: amendment filed on 3/3/06.

Withdrawn Rejections

3. Applicant has overcome the 35 U.S.C. 101 Rejection of claim 20 set forth in the previous Office Action by canceling said claim. Consequently, this rejection has been withdrawn by the examiner.

Maintained Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 21, 23, 25 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Avnon et al., U.S. Patent 5,559,977, herein referred to as Avnon.

6. As per claim 21, Avnon teaches a processor comprising:

-An integer pipeline process integer instructions: [*Integer pipeline, depicted in figure 4, IP3 and IP4. Column 7, lines 50-59]*

-A floating point pipeline to process floating point instructions, wherein the floating point pipeline has a greater number of pipeline stages to process floating point instructions than a number of pipeline stages to process integer instructions in the integer pipeline: having a second number of stages, which is greater than the first number of stages, to process floating point instructions: [*Floating Point pipeline, column 7, lines 35-65. Figure 4, IP1 and IP2]*

-And a control circuit coupled to the integer and floating point pipelines to inhibit co-issuance of an integer instruction to the integer pipeline when the integer instruction is subsequent to a first floating-point instruction in program order: [*The microvector sequencers 104u and 104v (figure 1) control the stalling of instructions issuance to both the integer and floating point pipelines. (Column 6, lines 51-65). This occurs when a second instruction (a floating point instruction within a pair of floating-point instructions) is determined to be a part of a pair of floating-point instructions that are unsafe. All subsequent integer instructions are stalled and not co-issued to the execution unit, which they otherwise would be, as two integer instructions can be co-issued under normal circumstances. For the issuing inhibiting see column 7, line 50 to column 8, line 9, column 9, lines 7-39 and column 6, line 51 to column 7, line 21. For normal issuing see figure 3, column 6, lines 30-39 and column 7, lines 22-3.]*

-Until the first floating point-instruction reaches a stage in the floating-point pipeline where exceptions are to be generated to ensure that the integer instruction does not graduate from the integer pipeline prior to exception

determination for the first floating point instruction in the floating-point pipeline,: [*Column 7, line 50 to column 8, line 9, column 9, lines 7-39 and column 6, line 51 to column 7, line 21. The subsequent integer instructions are not co-issued until the second instruction (unsafe floating point instruction within an unsafe floating point instruction pair) is deemed safe or it is handled.]*

-The control circuit to also inhibit co-issuance of a second floating-point instruction that follows the first floating-point instruction in program order, if the first floating-point instruction is not a short latency floating-point instruction, to ensure that the second floating-point instruction does not graduate prior to the exception determination for the first floating point instruction, but not to inhibit the second floating point instruction from co-issuance if the first floating-point instruction is a short latency floating-point instruction, since the second floating-point instruction will not graduate prior to the exception determination for the first floating-point instruction: [*Subsequent floating point instructions are also inhibited from co-issuance when the first floating-point instruction is an "unsafe" floating-point instruction. A safe floating-point instruction is a short latency floating-point instruction since it has been determined to be not an exception causing floating-point instruction. An unsafe floating-point instruction is not a short latency floating-point instruction since it can cause an exception, which will have a longer latency to handle than the safe floating-point instructions. Column 7, line 50 to column 8, line 9, column 9, lines 7-39 and column 6, line 51 to column 7, line 21.*]

7. As per claim 23, Avnon teaches the apparatus of claim 21 wherein the first floating-point instruction is a long latency floating-point instruction that has a longer latency period than the short latency floating-point instruction: *[A safe floating-point instruction is a short latency floating-point instruction since it has been determined to be not an exception causing floating-point instruction. An unsafe floating-point instruction is not a short latency floating-point instruction since it can cause an exception, which will have a longer latency to handle than the safe floating-point instructions. Column 7, line 50 to column 8, line 9, column 9, lines 7-39 and column 6, line 51 to column 7, line 21.]*

8. Given the similarities between claim 23 and claim 27, the arguments as stated for the rejection of claim 23 also apply to claim 27.

9. As per claim 24, Avnon teaches the apparatus of claim 21 further comprising a load/store pipeline coupled to the control circuit to process load and store instructions, the load/store pipeline also to be inhibited for co-issuance of load or store instruction, which is subsequent to the first floating-point instruction in program order, until the first floating-point instruction reaches the stage in the floating-point pipeline where exceptions are to be generated: *[Column 4, lines 27-65 and column 1, line 57 to column 2, line 2. The execution units 105u and 105v and address generators 106u and 106v, together execute load/store instructions, and therefore are a load/store pipeline. Also, the load/store pipeline uses the integer pipeline, and has the same stalling technique as the integer instructions.]*

10. Given the similarities between claim 24 and claim 28, the arguments as stated for the rejection of claim 24 also apply to claim 28.

11. As per claim 25, Avnon teaches a method comprising:

- Queuing a first floating-point instruction for issuance to a floating-point pipeline to process the first floating-point instruction: (Integer pipeline, depicted in figure 4, IP3 and IP4. Column 7, lines 50-59)

- Determining if exception handling for floating-point instructions is enabled: [*When the FIRC 201 performs "safe instruction recognition", it determines if the exception handling is enabled, because if an instruction is determined to be "safe", exceptions are guaranteed not to happen, thus, exception handling for that instruction is disabled. If an instruction is "unsafe", exception handling is enabled. Col. 9, lines 7-15]*

- Inhibiting co-issuance of an integer instruction to an integer pipeline when the integer instruction is subsequent to the first floating-point instruction in program order and the exception handling is enabled, until the first floating point-instruction reaches a stage in the floating-point pipeline where exceptions are to be generated to ensure that the integer instruction does not graduate from the integer pipeline prior to exception determination for the first floating point instruction in the floating-point pipeline: [(*Column 6, lines 51-65). This occurs when a second instruction (a floating point instruction within a pair of floating-point instructions) is determined to be a part of a pair of floating-point instructions that are unsafe. All subsequent integer instructions are stalled and not co-issued to the execution unit, which they otherwise would be, as two integer instructions can be co-issued under normal circumstances. For the issuing inhibiting see*

column 7, line 50 to column 8, line 9, column 9, lines 7-39 and column 6, line 51 to column 7, line 21. For normal issuing see figure 3, column 6, lines 30-39 and column 7, lines 22-3.]

- Determining if the first floating-point instruction is a short latency floating-point instruction: [*The FIRC 201 performs "safe instruction recognition". A safe floating-point instruction is a short latency floating-point instruction since it has been determined to be not an exception causing floating-point instruction. An unsafe floating-point instruction is not a short latency floating-point instruction since it can cause an exception, which will have a longer latency to handle than the safe floating-point instructions.* Col. 9, lines 7-15]

- Inhibiting co-issuance of a second floating-point instruction that follows the first floating-point instruction in program order and the exception handling is enabled, if the first floating-point instruction is not a short latency floating-point instruction, to ensure that the second floating-point instruction does not graduate prior to the exception determination for the first floating point instruction, but not to inhibit the second floating point instruction from co-issuance if the first floating-point instruction is a short latency floating-point instruction, since the second floating-point instruction will not graduate prior to the exception determination for the first floating-point instruction: *[Subsequent floating point instructions are also inhibited from co-issuance when the first floating-point instruction is an "unsafe" floating-point instruction. A safe floating-point instruction is a short latency floating-point instruction since it has been determined to be not an exception causing floating-*

point instruction. An unsafe floating-point instruction is not a short latency floating-point instruction since it can cause an exception, which will have a longer latency to handle than the safe floating-point instructions. Column 7, line 50 to column 8, line 9, column 9, lines 7-39 and column 6, line 51 to column 7, line 21.]

Maintained Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 22, 24, 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Avnon et al., U.S. Patent 5,559,977, herein referred to as Avnon in view of Halfhill, "SiByte Reveals 64-Bit Core for NPUs."

14. As per claim 22, Avnon teaches the processor in claim 21, however fails to specifically teach wherein the first floating point instruction is a multiply-add instruction, that has a longer latency period than the short latency floating-point instruction.

15. Halfhill teaches wherein a floating point execution unit executes floating point multiply-add instructions. One of ordinary skill in the art would have recognized that adding the capability of a multiply-add instruction would advantageously expand the functionality of the floating point execution unit. When the system determines that the

floating-point multiply-add instruction is unsafe, it would have a longer latency period than the short latency floating-point instruction (safe floating-point instruction).

16. The added functionality would have provided one of ordinary skill in the art with the motivation to add the multiply-add instruction to the possible floating point instructions that care executable by the floating point execution unit. This would in turn cause the second instruction to be a floating point multiply-add instruction in some instances.

17. Given the similarities between claim 22 and claim 26, the arguments as stated for the rejection of claim 22 also apply to claim 26.

Response to Arguments

18. Applicants arguments filed on 3/3/06 have been fully considered but they are not persuasive.

19. Applicant argues the novelty/rejection of the independent claims 21 and 25.

"Applicant submits that Avnon may teach integer and floating pipelines, in which stalls occur when floating-point instructions are determined to be unsafe. However, Avnon does not disclose the differentiation between short latency floating-point instructions and other floating-point instructions having longer latency. As stated in claims 21 and 25, co-issuance of a second floating-point instruction that follows the first floating-point instruction in program order is inhibited, if the first floating-point instruction is not a short latency floating-point instruction, but not inhibited from co-issuance if the first floating-point instruction is a short latency floating-point instruction.

20. These arguments are not found persuasive for the following reasons:

a. To clarify, floating point instructions and integer instructions are inhibited from co-issuance when the first floating-point instruction is an "unsafe" floating-point instruction. A safe floating-point instruction is a short latency floating-point

instruction since it has been determined to be not an exception causing floating-point instruction. An unsafe floating-point instruction is not a short latency floating-point instruction since it can cause an exception, which will have a longer latency to handle than the safe floating-point instructions. The FIRC 201 determines whether or not a floating-point instruction is "safe" or "unsafe". Column 7, line 50 to column 8, line 9, column 9, lines 7-39 and column 6, line 51 to column 7, line 21.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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